SIGMA-DELTA CONVERTER DATA-SHEET

Model's name:	SIGMA-DELTA CONVERTER
Short description:	1st up to 3rd order Sigma-Delta Analogue to Digital Converter
Archive's name:	michal_szermer.zip
Author's name (s):	Michal Szermer
Validated by:	
Repository date:	05.05.2004
Bibliographic reference(s):	A.S. Botha, P. Sniatala "HDL-A description of a/d converter based on delta-sigma modulator", *9th MIXDES conference, Wrocław, 2002, pp. 447-451* R. Baraniecki "Makromodele VHDL dla ukladow analogowo-cyfrowych" *Ph.D. thesis, Instytut Technologii Elektronowej, Warszawa 1998*
Name of the project:	Top Behav' Model'04
Computer type:	PC
Operating system:	Windows XP
Version:	2002
Simulation tool:	ADVanceMS (Mentor Graphics), version SV2002.0.10

	Name	***Version***
Entity name:	test_1st_order_sdc, test_2nd_order_sdc, test_3rd_order_sdc,	1.0
Architecture 1:	functional	1.0
Architecture 2:	behavioural	1.0

Function description:
I modelled 1st up to 3rd order SDC. In entity test_1st_order_sdc the 1st order SDC (modulator and decimator) are placed with input signal and clocks signals. In entity test_2nd_order_sdc the 2nd order SDC are placed, in entity test_3rd_order_sdc the 3rd order SDC are placed.

Validity domain:

Model interface:

Generics

Name	***Type***	***Description***
…	…	…
…	…	…

Ports

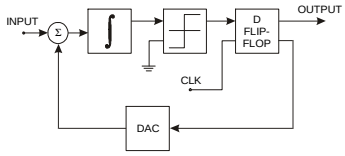
Name	Type	Class	Mode	Description
input	electrical			SDC input
AndInput	bit			Modulator output (decimator input)
outVector	bit_vector			12-bit digital output of SDC
clk	bit			internal clock
en	bit			enable signal of register
reset	bit			reset signal of counter
rst	bit			global reset

Others ports are internal nodes between components of the Sigma-Delta Converter.

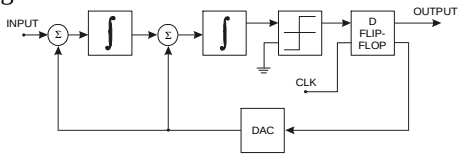
Model structure:

Block-diagram:

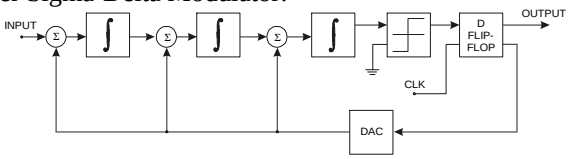
1st order Sigma-Delta Modulator:



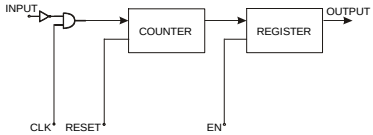
2nd order Sigma-Delta Modulator:



3rd order Sigma-Delta Modulator:



12-bit Decimator:



Hierarchy:

Model name	***Version***	***File names***

Package description:

1. In file sigma_delta.vhd all blocks of the SDC are placed.
2. In file signals.vhd all signals are placed
3. In file test1.vhd - 1st order SDC are described
4. In file test2.vhd - 2nd order SDC are described
5. In file test3.vhd - 3rd order SDC are described

Format of associated files: *.vhd (test files), *.txt, *.cmd and *.ps

Electrical characteristics: …
Dynamical characteristics (time/frequency) …
Parameter to identify: …

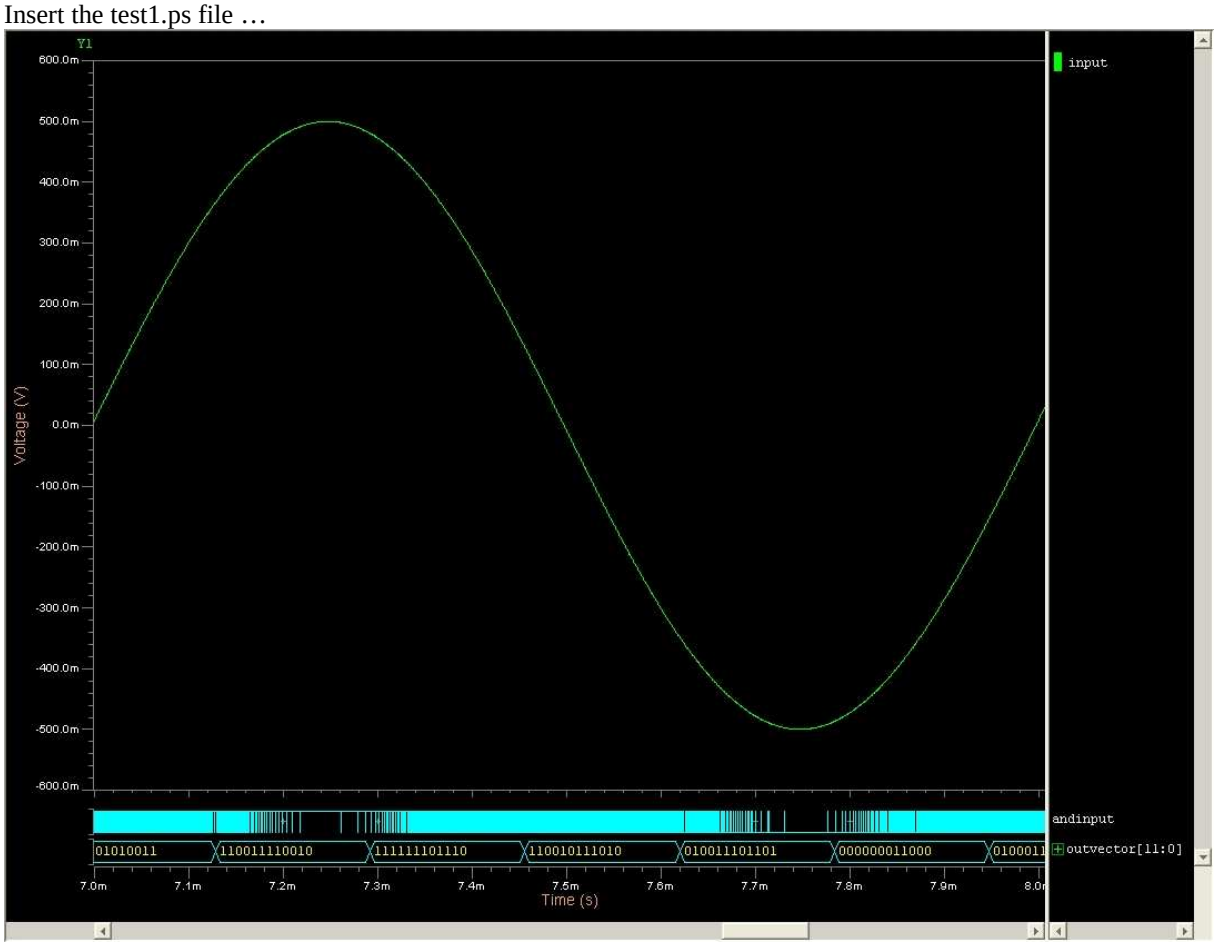
Absolute maximum ratings: …
Recommended operating conditions: …

Tests description:

Test 1: **work conditions:**

Input: input
Settings: Time-Domain Analysis:
Time Start: 0, Time Stop: 10m, Time Step: 1n
Outputs: andinput, outvector[11:0]

Insert the test1.ps file …



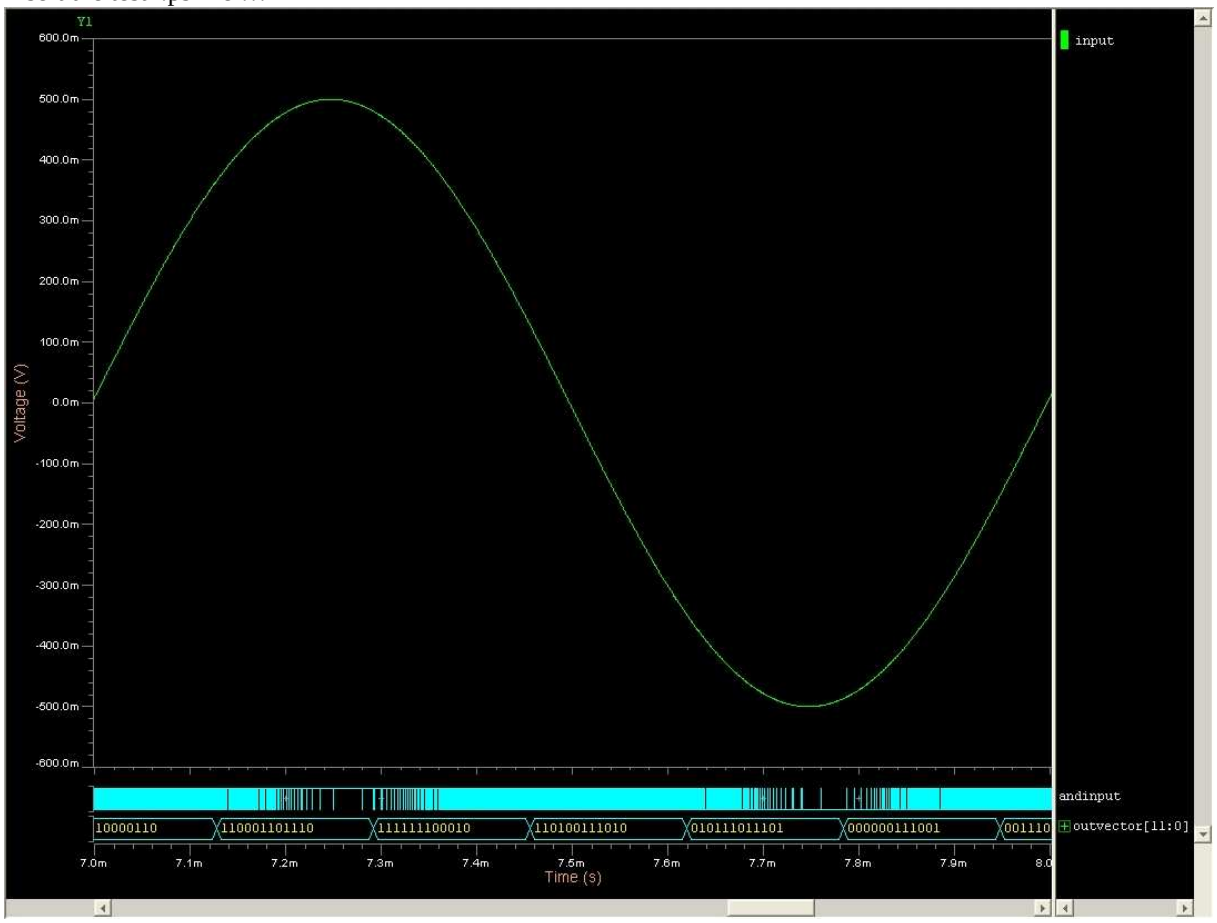
Curves comments …

1. input - input signal of the sigma-delta converter
2. andinput - output of the sigma-delta modulator (decimator input signal)
3. outvector[11:0] - 12-bit digital output word of the 1st order sigma-delta converter

Test 2: **work conditions: …**

Input: input
Settings: Time-Domain Analysis:
Time Start: 0, Time Stop: 10m, Time Step: 1n
Outputs: andinput, outvector[11:0]

Insert the test2.ps file …



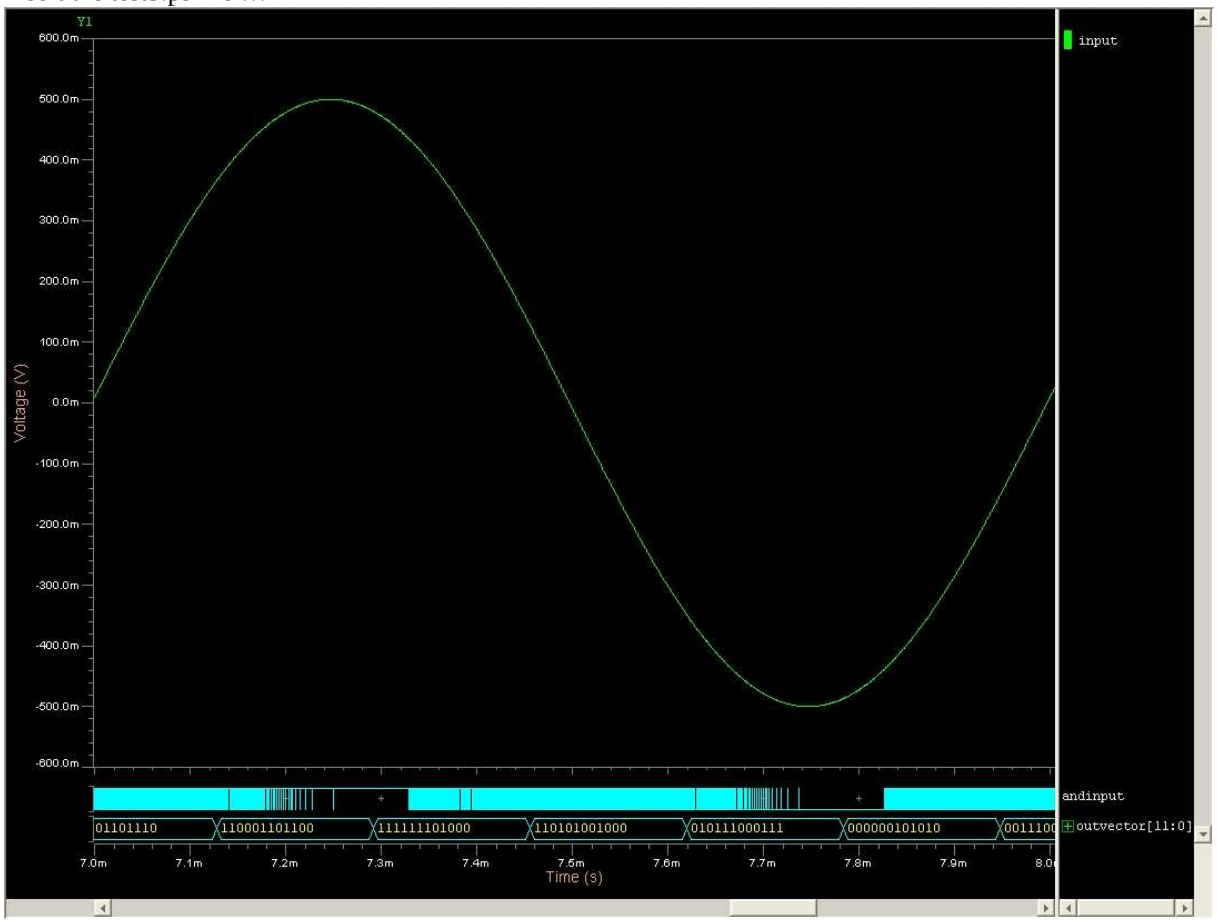
Curves comments …

1. input - input signal of the sigma-delta converter
2. andinput - output of the sigma-delta modulator (decimator input signal)
3. outvector[11:0] - 12-bit digital output word of the 2nd order sigma-delta converter

Test 3: **work conditions: …**

Input: input
Settings: Time-Domain Analysis:
Time Start: 0, Time Stop: 10m, Time Step: 1n
Outputs: andinput, outvector[11:0]

Insert the test3.ps file …



Curves comments …

1. input - input signal of the sigma-delta converter
2. andinput - output of the sigma-delta modulator (decimator input signal)
3. outvector[11:0] - 12-bit digital output word of the 3rd order sigma-delta converter

Application notes: …
Known bugs and limitations: Exceeded capacity limit of 30 quantities for Educational edition!

History:

Old Version	*New Version*	*Modified by*	*Change(s)*
No	0.9		

Archive content:

Author_name/ Michal_Szermer

Model/	sigma_delta.vhd signals.vhd data-sheet04.doc
Test1/	test1.vhd test1.txt test_1st_order_sdc.cmd test1.jpg
Test2/	test2.vhd test2.txt test_2nd_order_sdc.cmd test2.jpg
Test3/	test3.vhd test3.txt test_3rd_order_sdc.cmd test3.jpg

Ideas to follow:

Acknowledgements:
The author wish to thank M.Sc. Rafal Kielbik from Department of Microelectronic and Computer Science at Technical University of Lodz for kind sharing of information on his research results related to designing sigma–delta analog to digital converters.
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