9th International Conference

MIXED DESIGN

MIXDES 2002
Wrocław, POLAND
20 – 22 June 2002

TECHNOLOGY AND MEASUREMENTS OF BACKSIDE CONTACTED ISFETS

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KEYWORDS: ISFETs, Semiconductive Sensors, Miniaturized Sensors

ABSTRACT: An approach of Ion Sensitive Field Effect Transistor (ISFET) structures with a contact pads located at the back – passive side of the structure is presented. It has been found that high linearity of measured V_{GS} signal versus pH values in the range 2-12pH requires that the ISFETs are measured at U_{DS}=0,5V and I_D=0,1mA in the constant current configuration. The chip assembling is to be performed in very simple and quick manner applying special designed self-clamping head with the telescope pins (designed and manufactured by the Technical University of Warsaw at Chemical Dept.).

INTRODUCTION

The concept of assembling of Ion Sensitive Field Effect Transistor (ISFET) structures with a contact pads located at the back – passive side of the structure, facilitates considerably protection of the structure against chemically aggressive environment and makes exchange of the structure in field condition much easier. This approach however poses difficult technological requirements. To ensure the electrical connection throughout the silicon wafer thickness over 300 μm deep cavity has to be formed to reach a close vicinity of the active side of the device followed by deep diffusion throughout remaining silicon membrane. Next, this deep cavity has to be effectively coated with continuous metal film which form a contact pad to external connector. Coating and structuring of such 3-D structures requires special technological endeavours. The procedure of manufacturing of the ISFET structures with such backside contacts is following:

PROCEDURES

Double-side polished silicon wafers (3", n-type, <100> oriented, 5-8 ? cm resistivity and 380 μm thick) have been used to manufacture the device. A cross section of an ISFET with backside contacts developed by Institute of Electron Technology is shown in Fig.1.

The ISFET chip shown at its bottom view – Fig. 2, has two aluminium electrodes (formed over the cavities) to the source and drain areas respectively.
The source (n^+) is short circuited with the p-type substrate by the metalization for proper device biasing. To form the cavities an anisotropic etching of silicon in KOH solution has been performed at the back side of the wafer as one of the first technological steps. This etching is performed leaving 30 μm thick membranes.

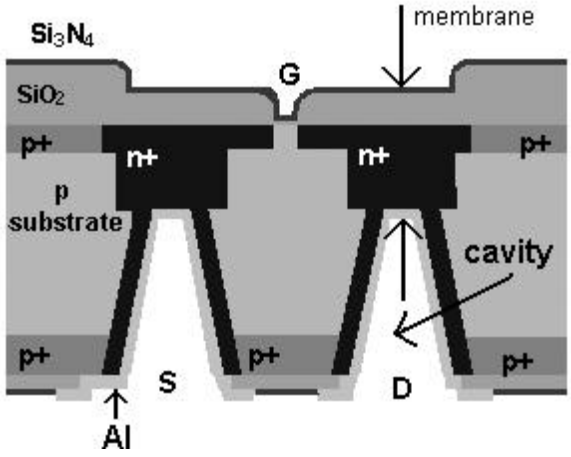

Figure 1. *The cross section of an ISFET with backside Al contacts*

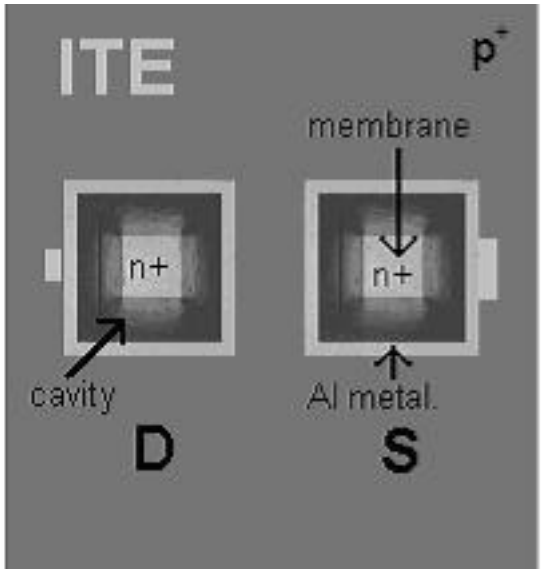

Figure 2. *The ISFET chip - its bottom view with a pair of the Al metalized cavities (Drain and Source electrodes)*

Next, the membranes are n^+ doped from its both sides by the deep phosphorus diffusion to make good electric contacts to the source and drain areas of the device. It has to be noted, that due to the fact, that formation of the backside contact cavity and diffusion connection requires both (consecutive), aggressive chemical and long-term high temperature treatments, it has to be performed before manufacturing of the ISFET structure. Thus, special precautions have to be undertaken to protect the silicon wafers with delicate, thin silicon membranes during the rest of the processing sequence. The main ISFET structure is built at the front side (Fig.3) of the wafer by applying ion implantations (n^+-doped source and drain areas, n^+-doped channel gate, p^+-doped channel stoppers), 9 photolithography levels, silicon dioxide and silicon nitride layers depositions and local oxidations (LOCOS) as commonly used in MOS technology. The transistor has n-type built-in channel and the device works in depletion mode.

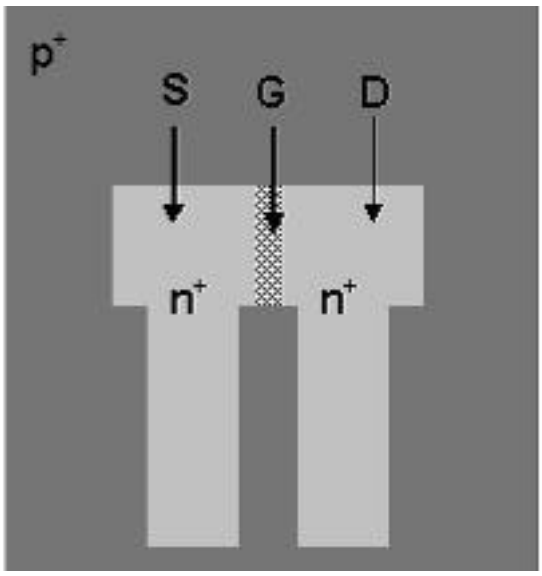

Figure 3. *The ISFET chip - its front view topology with marked areas of Source, Drain and Gate*

The dielectric gate (ion detection area) composes of thin silicon oxide and silicon nitride layers. The ISFET structure with such a gate may be directly used for pH measurement in the range 1-12 pH. Selective measurement of concentration of different ions is possible by deposition of a "poliHEMA" layer followed by additional ion selective film on the gate area. The chip assembling is to be performed in very simple and quick manner applying special designed self-clamping head with the telescope pins (designed and manufactured by the Technical University of Warsaw at Chemical Dept.).

RESULTS

The ISFETs have been measured and preliminary characterised in the IET R&D facility using the Keithley 236/237 Source Measure Unit. The ISFETs output characteristics I_D versus U_{DS} have been plotted (see Fig. 4) for the two test pH solutions (pH 4 and 9). In this figure drain current I_D decreases with increase of the pH.

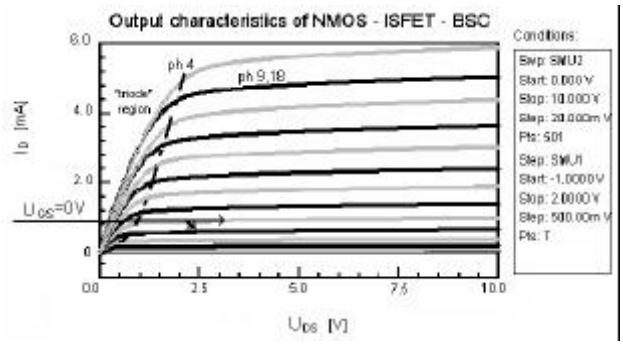

Figure 4. *The ISFET Output characteristics $I_D(U_{DS})$ at pH 7 and pH 9.18*

It has been found that high linearity of measured V_{GS} signal versus pH values in the range pH 2-12 requires that the ISFETs are measured at U_{DS}=0,5V and I_D=0,1mA in the constant current configuration. This bias operating point is within 'triode' region (called also a linear one) of the output characteristics shown in Fig. 4.

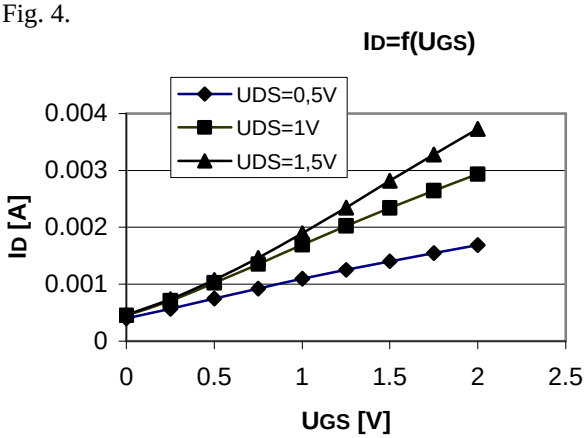

Figure 5. *The $I_D(U_{GS})$ characteristics at U_{DS}=0,5V, 1V, 1,5V and pH 9.18*

As it is seen from the Fig. 5 an operating point of U_{DS}=0,5V gives the best linearity of V_{GS} (pH). The $I_D(U_{GS})$ transfer characteristics have been plotted for three pH values: 4.00, 7.00, and 9.18 (see Fig. 6).

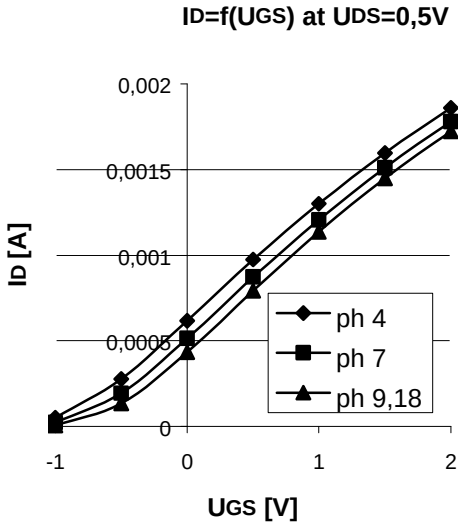

Figure 6. *The ISFETs transfer characteristics $I_D(U_{GS})$ at U_{DS}=0,5V and pH values: 4, 7, 9.18*

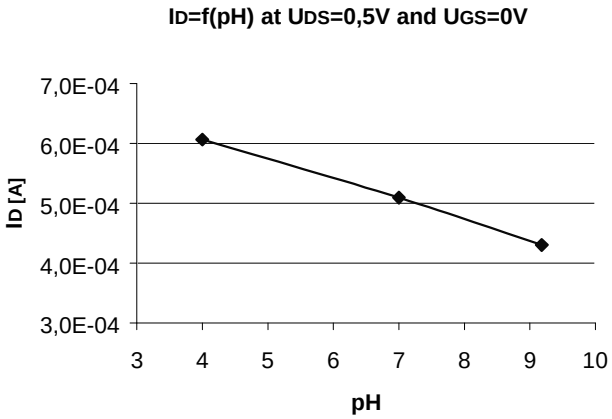

Figure 7. *The I_D versus pH at U_{DS}=0,5V and U_{GS}=0V*

The I_D (pH) dependence is shown in Fig. 7. The curve from Fig.7 has good linearity and slope for pH measurements.

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ACKNOWLEDGMENTS

This work was supported by the European FP 5 Project "SEWING", contract no.: IST-2000-28084.