

Modelling, Simulation and Design Sigma-Delta Converters in Silicon Microsystems

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Abstract – The purpose of this paper is the new approach of modeling and designs the sigma-delta converters in silicon microsystems. Microsystem described in this paper bases on two major parts. First part consists of various sensors and the second part consists of analogue to digital converters as well as other standard electronics circuits. The analogue to digital conversion is performed using sigma – delta modulators. Modulators were designed in CAD CADENCE environment and simulated using SPECTRES, and ELDO simulators. In this paper the simulation results were presented, and discussion of the advantages of sigma-delta conversion in this kind of measurement was underlined.

Keywords - sigma-delta modulator, silicon microsystem, CADENCE, SYNOPSIS, ELDO.

I. INTRODUCTION

During last years an increase in interest of silicon microsystem has been denoted. They can be more often found in many different industrial realisations. The development was possible due to new micromachine technologies, which allow making etched areas in silicon bulk. Over an etched area a silicon bridge is expanded. The principle of operation is based on controlled heat transfer along the bridge that contacts the bulk on its ends. On the bridge a whole variety of microsensors (e.g. temperature, pressure, and infrared radiation) can be placed. The size of these sensors is very small (thousands of micrometers) so they are extremely sensitive on changing of measured value. To obtain the results of the measurement the external noise should be minimised. This can be obtain by using module that converts analogue signals into digital, which is much more resistant to external interference and can be easily used in further computer calculations. For proper designing of silicon microsystem, specialised CAD software is needed i.e. CADENCE, which allows designing a scheme and layout of the microsystem and simulation of A/D converters. It is also necessary to use ELDO simulator for appropriate modelling the whole microsystem.

II. SILICON MICROSYSTEM

In Department of Microelectronics and Computer Science at Technical University of Lodz, silicon microsystems were designed by using specialised CAD software. The second generation had an implementation of sensors and A/D converters “on chip”. This chip consists of two parts. First is

the MEMS (Micro-Electro-Mechanical-Structure) unit encloses a set of sensors. The design path is not so complicated. Firstly parameterised cells of certain sensors were created. Secondly cells were collected in a library file, so a sensor of a certain parameters can be further easily designed. Finally, using previously designed cells, a set of microsensors was created. In that way a MEMS unit of microsystem was designed. The data processing unit was created very similar way, by using a layout editor and schematic editor in CADENCE software. This part consists of the sigma-delta modulator and decimation filter. The block scheme is presented on fig.1.

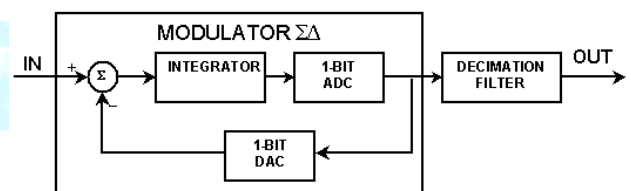


Fig.1. Block diagram of the data processing unit

Moreover sigma-delta modulator consists of integrator 1-bit analogue to digital converter and 1-bit digital to analogue converter. This is the simplest configuration of this converter. The data processing unit was designed in CADENCE schematic editor and simulated by using SPECTRES simulator. The results of simulations were presented in this paper.

III. MODELLING OF THE SIGMA-DELTA MODULATORS

As it was mentioned in the previous part of this paper the second crucial part of presented microsystem is data processing unit. It consists of sigma-delta modulators and decimation filter. All parts of mentioned above were designed in CADENCE schematic editor tool. To simulate microsystem models of sigma-delta modulator were performed in SPICE and tested in multidomain ELDO simulation program. The two modulators were tested. All were realised in SC techniques. First one was as a first order modulator and the second one was as a second order modulator. The electrical scheme of simulated modulator was presented on fig.2.

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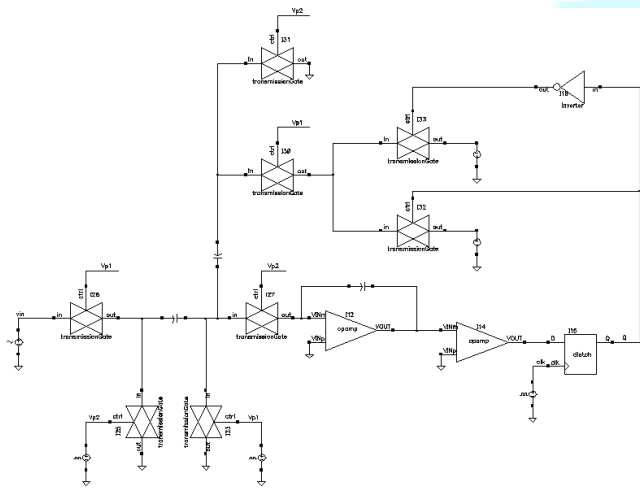


Fig.2. Electrical scheme of the first order switched capacitor modulator

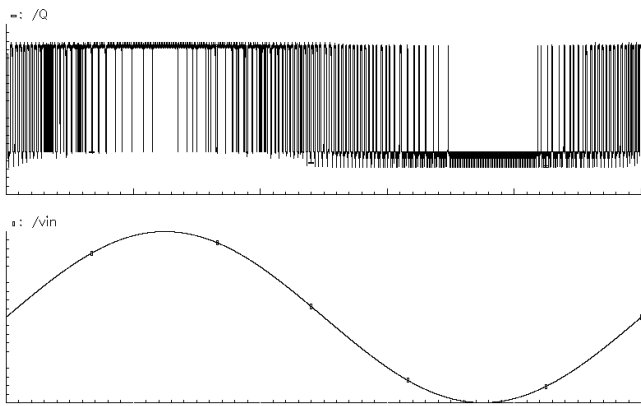


Fig.3. Input and output signals of sigma-delta modulator

The simulation results of first order sigma-delta modulator was presented on fig.3. Using modulators the analogue signal is changed in frequency modulated signal. That is why the external interference on analogue signal is minimised.

IV. DESIGN AND SIMULATION OF THE DATA PROCESSING UNIT

The second part of microsystem can be divided into two separate parts. The first part of circuit is a sigma-delta modulator presented in previous chapter. The second part of data processing unit is decimation filter. This circuit is necessary to create digital output word. The filter was described in VHDL language, which is dedicated to design digital circuits. Next step was designed and verification in SYNOPSIS software. Last step was layout generation by using CADENCE environment. The full design flow was presented on fig. 4.

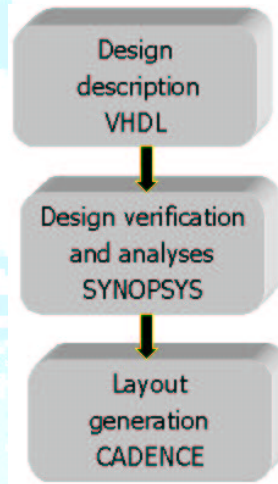


Fig.4. Design path of decimation filter

The description of a part of decimation filter of data processing unit in VHDL language is presented below.

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity ascount is
  port (clk, areset, sreset, enable: std_logic;
        count: buffer unsigned(3 downto 0));
end ascount;

architecture archascount of ascount is
begin
  p1: process(clk, areset, sreset, enable) begin
    if (areset = '1') then
      count <= (others => '0');
    elsif (clk'event and clk = '1') then
      if (sreset = '1') then
        count <= (others => '0');
      elsif (enable = '1') then
        count <= count + 1;
      else
        count <= count;
      end if;
    end if;
  end process;
end archascount;

```

Fig.5. Description of decimation filter in VHDL language

The behaviour of the circuits was described in VHDL language. The next of design path requires schematic generation. It is obtained with usage of SYNOPSIS environment. The results of this are presented on fig.6.

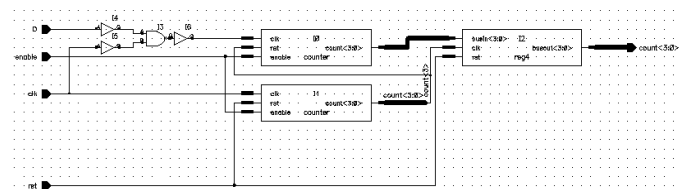


Fig.6. Electrical scheme of the decimation filter

The last step was to connect modulator and decimation filter using CADENCE schematic editor. In this way the whole data processing unit was designed.

V. CONCLUSIONS

The silicon microsystem presented in this paper had been fully designed in CADENCE environment. Using SPECTRES simulator the data processing unit was simulated. Results of the simulations were presented on this paper. There are also library files that include basic electronic cells as symbol schematics; layouts and models were created. The main aim of this work was to simplify design process of the integrated circuits.

VI. ACKNOWLEDGEMENTS

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