

LABORATORY MEASUREMENT STAND OF ANALOGUE TO DIGITAL CONVERTERS WITH APPLICATION OF LABVIEW ENVIRONMENT

M. SZERMER, P. PIETRZAK, M. DANIEL, A. NAPIERALSKI
TECHNICAL UNIVERSITY OF LODZ, POLAND

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ABSTRACT: This paper describes measurement stand dedicated to analogue to digital converters. The tested ADC is sigma-delta converter with adjustable configuration. The first part of the paper concerns the structure of the converter and simulation results. Further, the dedicated laboratory measurement stand is described. It consists of the test PCB board connected with data acquisition PC board NI6025E and PC Workstation with LABVIEW environment installed. The whole measurement system can be managed from the GUI designed by the authors in order to provide efficient measurement and its automatization. In this paper advantages and disadvantages of this kind of measurements are discussed.

INTRODUCTION

The aim of V European Project (SEWING) is to create silicon microsystem dedicated to water pollution monitoring. This system consists of chemical sensors such as ISFET/CHEMFET described in [2],[3], and processing part. The crucial part of the processing unit is analogue to digital converter. After intensive research on appropriate choice of this kind of circuit, the sigma-delta converter with adjustable configuration was chosen [9]. Thanks to this the accuracy of the signal conversion according to the project requirements can be adjusted. The main aim of elaborating such a structure was to choose the best possible ADC for the purpose of sensor signal processing. As a final result, designed ADC is to be the part of microsystem that incorporates standard electronic units together with sensors and its operating circuits.

Next section gives brief outline of designed ASIC – AD Converter

SIGMA-DELTA ANALOGUE TO DIGITAL CONVERTER

In this part of the paper the basic concept of the modular structure of the sigma-delta converter is presented [1],[5],[10]. Designed sigma-delta converter contains of two parts:

- Sigma-Delta Modulator
- Decimator

The first part is designed as a modular structure of adjustable configuration. One of two following configuration can be set up by the user:

- Serial Integrators Connection
- Triple First Order Cascade (MASH 1-1-1)

It is also possible to set up the proper structure of Serial Integrators Connection by choosing the number of integrators connected in series:

- 1st order SDC
- 2nd order SDC
- 3rd order SDC
- 4th order SDC

Configuration flexibility gives an opportunity of testing and comparison up to five different structures of ADC. The block diagram of the AD converter is presented in Figure 1.

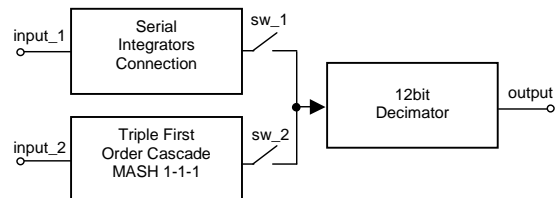


Fig.1. Modular structure of the sigma–delta converter

All of the parts of the converter are designed with application of VHDL–AMS language with application of behavioural description [4],[8]. Moreover, the simulation of the whole microsystem (chemical sensors ISFET/CHEMFET and processing part) becomes possible.

Simulation the whole of the converter with application of VHDL–AMS simulator lasts about 30 minutes, so it reduces the entire simulation time and enabled to perform the simulation of various different configurations of ADC. These fast high-level simulations made possible to choose the most promising configuration. Afterwards, the best solution was implemented in SPECTRES, and CADENCE.

The electrical scheme and layout was created in CADENCE environment. Accurate simulation of the ADC with application of very detailed technology-

related models performed in SPECTERS took about 30 hours. On the basis of this accurate simulation the layout was generated. The layout of designed modular structure of the sigma-delta converter is presented in Figure 2. The whole project was created in the Department of Microelectronics and Computer Science in Technical University of Lodz with application of proper software. To modelled SDC in VHDL-AMS language the hAMStor software was chosen. After behavioural simulations the SDC was designed as an ASIC with application of CADENCE environment. Before the manufacturing phase of the AD converter post-layout simulations had to be performed. The next section presents the simulation results of investigated structures of ADC.

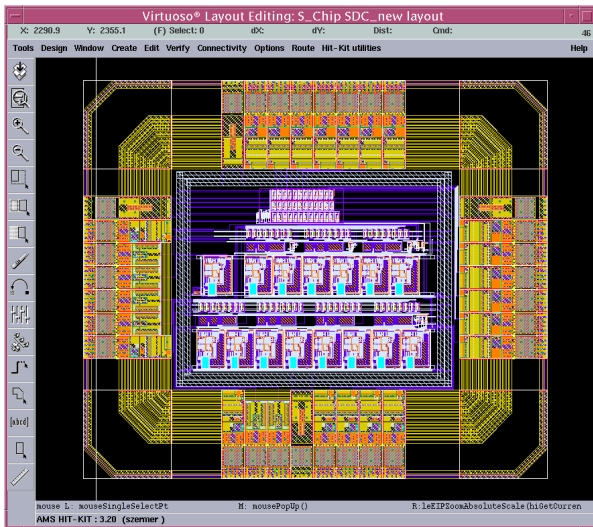


Fig.2. Layout of the modular structure of the sigma-delta converter

SIMULATION RESULTS

To estimate which configuration offers the best possible performance it was necessary to take some criteria of comparison. To achieve this two main parameters are calculated and compared:

- Signal to Noise Ratio (SNR)
- Total Harmonic Distortion (THD)

To define these parameters the FFT of the output signal had to be calculated. Figure 3 shows the results the FFT analysis of the second order sigma-delta converter.

As can be seen in the spectrum a single line for the main frequency of the input signal is visible. Remaining harmonics of the signal are damped.

Figures 4 and 5 show the SNR dependence on input signal level for the case of serial integrator connections and triple cascade of the converter respectively.

As can be seen for 1st order SDC (Figure 4) this characteristic shows linear dependence in whole range. For the 2nd and 3rd order SDC obtained characteristic are linear for the input signal equal -10dB to 0dB. In the lower range characteristic resembles square dependence on input signal level. For the 4th order sigma-delta converter is unstable and is not further discussed.

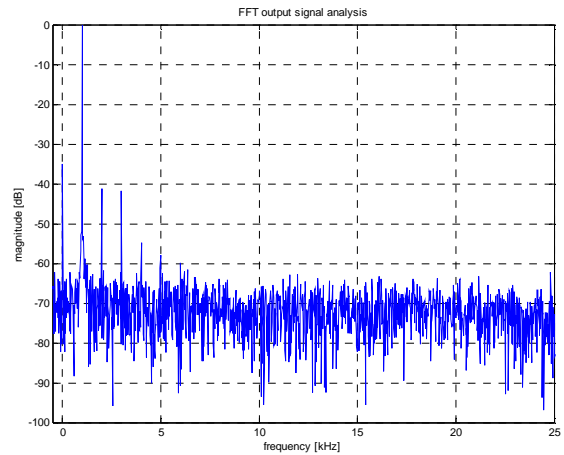


Fig.3. FFT transform of the output signal of the 2nd order SDC

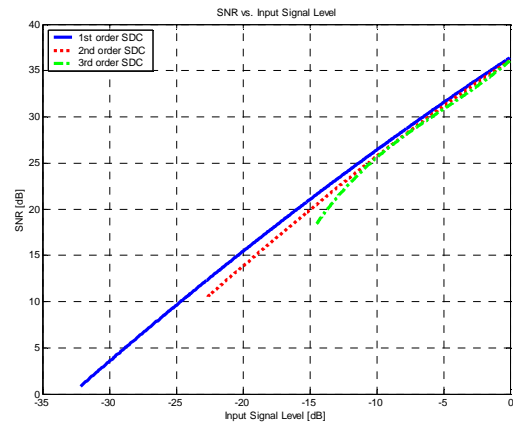


Fig.4. SNR vs. Input Signal Level of the serial integrator connections of the 1st, 2nd, 3rd order SDC

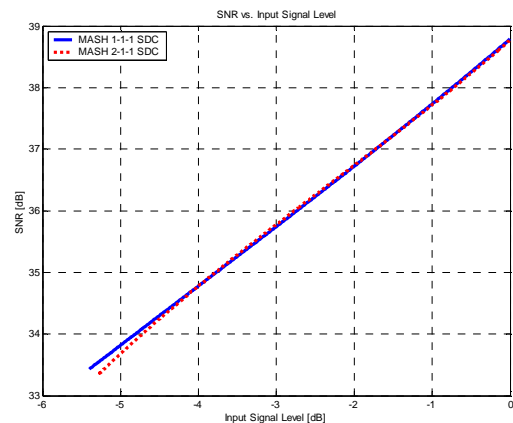


Fig.5. SNR vs. Input Signal Level of the serial integrator connections of the MASH 1-1-1 and MASH 2-1-1 SDC

The characteristics of two investigated cascade structures - MASH 1-1-1 as well as MASH 2-1-1 are demonstrated too (Figure 5). For both cases the SNR dependence on input signal level resembles linear. In table 1 calculated values of THD and SNR are demonstrated which refers to all investigated ADC

structures. The coefficients values were calculated for the test signal of 1kHz covering full processing range of the entities.

Table 1. SNR and THD for the investigated sigma-delta converter

	1st	2nd	3rd	MASH 1-1-1	MASH 2-1-1
SNR [dB]	36.55	36.41	36.13	38.75	38.72
THD [dB]	-38.34	-38.53	-37.88	-36.58	-37.02

Analysis of calculated coefficients values (table 1) shows, that all configurations of the sigma-delta converters demonstrate comparable performance.

TEST CHIP OF THE SIGMA-DELTA ANALOGUE TO DIGITAL CONVERTER

Discussed structures of converters are manufactured as ASIC in AMS 0.6 μ m CMOS technology and demonstrated in Figure 6. This chip is designed with application of CADENCE environment. The photo of the fabricated chip is presented in Figure 6. It occupies 4.2 mm² area and dissipates the power of 16 mW.

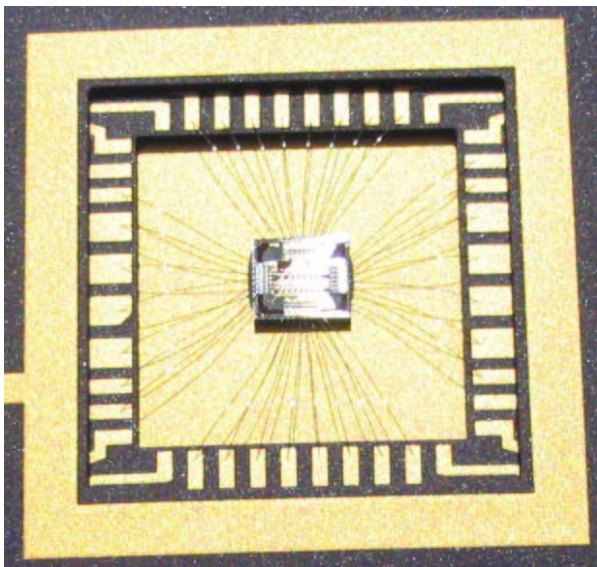


Fig.6. The photo of the fabricated chip

To ensure precise and reliable measurements the dedicated measurement stand was designed. The next section gives detailed characteristic of designed measurement stand.

MEASUREMENT STAND FOR ANALOGUE TO DIGITAL CONVERTERS

After short presentation of the basic concept of the sigma-delta converter and simulation results, in this paragraph special measurement stand are described. Hardware of the proposed testing stand for Analogue-to-Digital converters consists of ADC board and personal

computer equipped with one of the National Instrument measurement card [6],[7]. The block diagram of the measurement system is presented in Figure 7.

The main part of the measurement board is tested ADC. The whole system can be divided into several circuits that deliver required signals to the ADC and connect its output with the measurement card installed in the PC. Two channel or multiplexed input ADCs can be tested using presented board. It is achieved by double input signal circuits on the board.

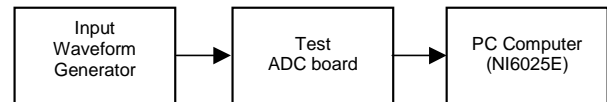


Fig.7. Block diagram of the whole measurement system

The block diagram of the ADC board is shown below.

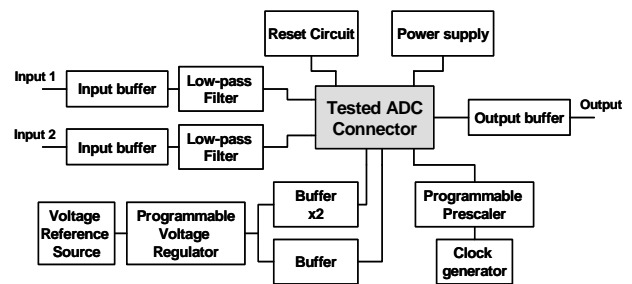


Fig.8. Block diagram of the ADC Board

Each input channel consists of buffer and a simple RC low-pass filter. As a buffer the rail-to-rail input/output, single supply, low noise (5nV/ $\sqrt{\text{Hz}}$), and high-speed (38MHz, 22V/ μ s) operational amplifier OPA2350 by Burr Brown was used. Completely independence of each circuit in the dual amplifier chip minimizes crosstalk and internal interaction. Feature of this ICs make them ideal for driving Analogue-to-Digital Converters. The buffers ensure that the DAC input voltage does not exceed supply voltage value and drive filter circuit.

To improve functionality of the board and make it possible to test ADCs in various conditions programmable reference voltage was elaborated. It consists of reference diode and 8-bit Digital-to-Analogue Converter.

In the presented circuit the R-2R ladder of the DAC operates as a voltage-switching network. As a result from above picture, the reference voltage source is connected to one of the current output terminals (IOUT1 for true binary digital control, IOUT2 is for complementary binary). In this solution the reference voltage diode is biased through the DAC internal feedback resistor. The output voltage is taken from the normal VREF pin.

It is important that the voltage connected to the DAC output pin must be positive. When it went negative, the DAC output internal parasitic diodes (from ground to the OUT1 and OUT2) would turn on.

The ladder switches are voltage-controlled elements. When the DAC ladder works in the voltage-switching mode there is a dependence of conversion linearity and gain error on the voltage difference between VCC and the voltage applied to the normal current output terminals. To ensure that all 8 switches turn on sufficiently it is recommended that the applied reference voltage be kept less than +5VDC and the DAC supply voltage be at least 9V more positive than V_{ref} . The used 2,5V reference voltage source (with 12VDC DAC supply voltage) fulfills these restrictions and ensures less than 0.1% linearity and gain error change.

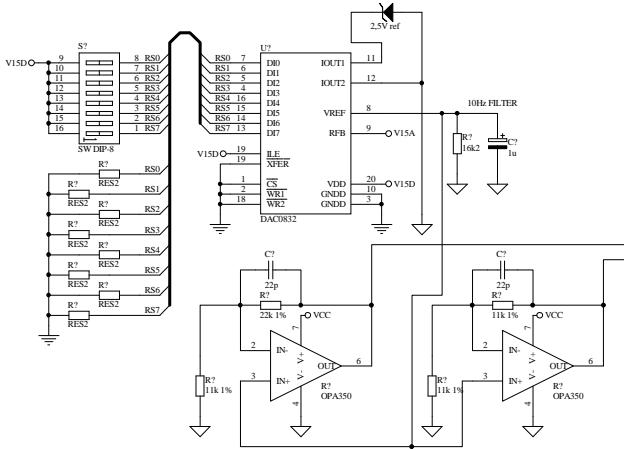


Fig.9. Programmable reference voltage source

The value of the output voltage is a function of the digital 8-bit word applied to the DAC and can change from 0V to 255/256 Vref:

$$V_{out} = V_{ref} \left(\frac{D}{256} \right) \quad (1)$$

where D – binary coded DAC input value.

Due to the fairly high output impedance of the DAC (10kΩ to 20kΩ) working in such configuration, it is recommended to use additional buffer. In that case in the above output voltage equation the value of the buffer gain must be taken into account. Then:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1} \right) \left(\frac{D}{256} \right) \quad (2)$$

where R_2 and R_1 are amplifier resistors.

Maximum conversion voltage of the Digital-to-Analogue Converter, the board was created for, depends on voltage connected to one of its pin. It was assumed that the value of this voltage should be twice higher than converter reference voltage level. This assumption is met by using two reference voltage buffers. One of them simply carries output voltage from the DAC, but second one doubles it.

The zero code output voltage of the DAC voltage regulator is limited by low level output saturation voltage of the opamps. The 2kΩ pull-down resistor helps to reduce this voltage.

One of the simplest and quite stable clock generators consist of TTL or CMOS gates and quartz oscillator. Due to problems with excitation the quartz crystals at their fundamental frequency, the maximum frequency of such generators is reduced to about 30MHz. In the presented solution, a parallel resonant circuit impels the 48MHz quartz-crystal resonator to oscillate at their third harmonic frequency. The second inverter buffers output signal from the first inverter. Both inverters must be unbuffered CMOS type. Used HCU series inverter allows the generator to work at 60MHz maximum frequency.

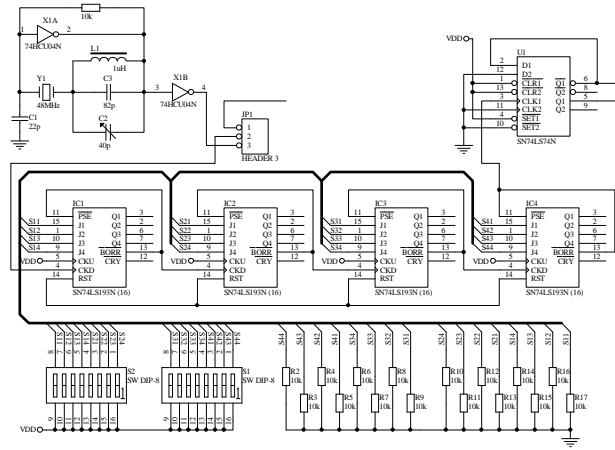


Fig.10. ADC Board Clock Generator

The frequency signal goes from generator to manually programmable 16-bit prescaler that is based on four 4-bit up/down counters with preset and carry/borrow outputs. All the counters count down and send “borrow” (BORR) signal to the following stage when the value exceed zero. To obtain 16-bit counter counting down from the initial value the “borrow” signal of the last (most significant 4 bits) counter should control load inputs of all prescaler counters. Such solution is impossible because of signal propagation delays of circuit. The worst case appears when the prescaler turn from the counted 0 value to the initial value.

For used 74F193 counters the signal propagation delay from the CKD to BORR pins should not exceed 8ns. Maximum delay time between the load control input PSE and counter flip-flops approximates 12ns. It means that the initial values of first counter will be loaded in about 44ns after the previous generator pulse - the signal has to go through the all counters and back to the first one as the load signal. After including PCB path propagation time we calculate, that prescaler input clock frequency must be lower than 18MHz.

The solution for this problem is using “local” load signal for each counter. In such case prescaler input frequency can reach at least 50MHz. Then, the output frequency is equal to:

$$F_{out} = \frac{48MHz}{2 \cdot (n(IC1)+1) \cdot (n(IC2)+1) \cdot (n(IC3)+1) \cdot (n(IC4)+1)} \quad (3)$$

where n(ICx) – x-counter preset values.

The last D flip-flop symmetries ADC clock signal and simultaneously divides the clock frequency by two. The ADC input frequency may be set in range of 366Hz to 24MHz. Additionally it is also possible to achieve clock signal from measurement card.

All the analogue and digital signals going to and from the tested ADC are buffered and delivered to proper inputs of the measurement card. It helps to display actual state of the ADC at the computer monitor. The tested ADC is additionally protected before improper measurement card configuration.

The power supply delivers separate voltages for analogue and digital circuits. The most popular 78XX series linear voltage regulators supply digital and the reference voltage circuits. Precise voltage regulator supplies the analogue part of the board.

Thanks to all-purpose solutions the most of market available Analogue-to-Digital Converters can be connected to the board using proper adapter. The whole system allows to quickly evaluating the performance of the tested ADC.

MEASUREMENT APPLICATION USING LABVIEW ENVIRONMENT

Presented measurement board cooperates with application written in LabVIEW environment [6]. In order to support efficient data acquisition process the dedicated Virtual Instrument (VI) was designed. Thanks to this measurement results can be easily process by application written in LabVIEW environment. Another function of mentioned VI is to provide online data processing and efficient results visualisation. The test board is connected with PC computer equipped in data acquisition card NI6025E. This card has 16 analogue channels, which are used for communication purposes with output signals of the designed sigma-delta converter. Data obtained from these channels are converted into bit stream and saved to the file.

Typical application written in LabVIEW environment can be dividing into two basic parts:

- Panel window
- Diagram window

The first window refers to visualization of the measurement results. The GUI of designed application is presented in Figure 12. Moreover from this window some parameters can be set.

The second application window contains code of the application. It consists of the library elements (virtual instruments) properly connected one to another.

In the panel window (Figure 12) the test signal of the converter in time and frequency domain is shown. This signal is process by sigma-delta converter and digital output word is saved in output file (this code of application is shown in diagram window).

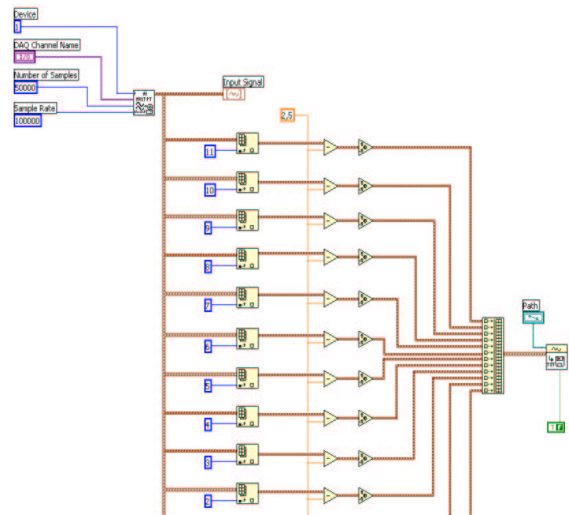


Fig.11. Diagram window of the application dedicated to measurement SDC

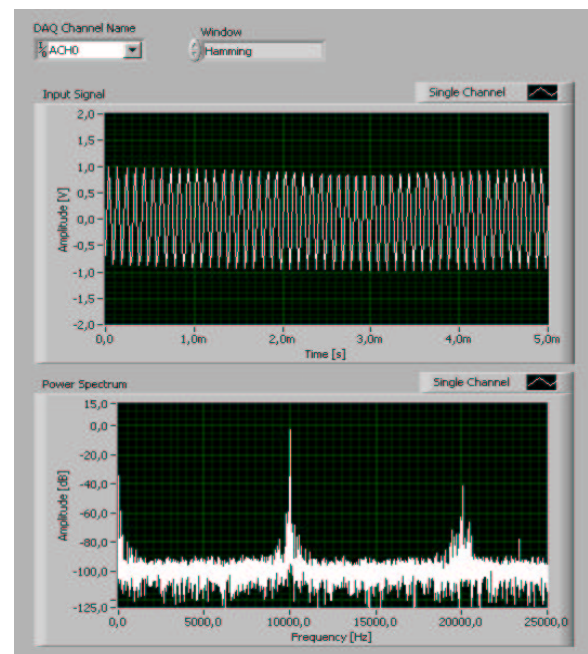


Fig.12. Panel window of the application dedicated to measurement SDC

CONCLUSIONS

In this paper the sigma-delta converter and special measurement stand are presented. The modular structure of the converter renders possible to adjust such a configuration of ADC that satisfies the end user requirements. The elaborated ADC structure makes also possible to adjust the effective digital resolution of the ADC. In order to provide efficient, automatic measurements of this circuit the special measurement stand was designed. It provides not only the stable and precise signals to the tested entity but also enables to attractive measurement results visualisation as well as fast and efficient data acquisition. The main advantage of this solution is that it required standard electronics component mounted on PCB board with test circuit. With application of digital prescaler a wide range of

clock frequency can be applied to the test circuit. It is easy to define maximum clock frequency with which sigma-delta converter can proper operate.

On the basis of described measurement system the wide range of configurations of the sigma-delta converter will be tested. After the test phase the best possible configuration and resolution will be chosen. It will be come also the base of further research on possibilities of integration of processing unit on-chip with ISFET/CHEMFET sensors as well as its operating circuitry.

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THE AUTHORS

Michal Szermer and Piotr Pietrzak are the Ph.D. students of the Department of Microelectronics & Computer Science, Technical University of Lodz, Poland.

Ph.D. Marcin Daniel is a research/teaching staff of the Department of Microelectronics & Computer Science, Technical University of Lodz, Poland.

Prof. Andrzej Napieralski is the Head of the Department of Microelectronics & Computer Science, Technical University of Lodz, Al. Politechniki 11, 93-590 Lodz, Poland

E-mail: szermer@dmcs.p.lodz.pl

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